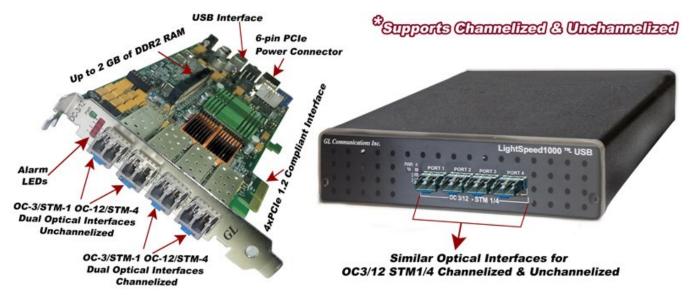
LightSpeed1000[™](w/ GigE and USB 2.0) (Legacy Product)

(OC-3/STM-1, OC-12/STM-4 Analysis and Emulation Card)



Overview

GL's LightSpeed1000[™] hardware platform (available as PCIe Card and USB Pod) is capable of OC-3/12 and STM-1/4 wirespeed processing on quad optical ports for functions such as wirespeed recording and wirespeed playback of Unchannelized and Channelized ATM, PoS, RAW Traffic. Two ports out of the 4 ports are meant for SONET/SDH unchannelized and unframed data. The remaining two ports are meant for SONET/SDH channelized data of carrying many independent unframed/framed T1, E1, T3, and E3 streams

The LightSpeed1000[™] comes with software for overall monitoring, BERT, emulation, and protocol analysis with a price tag that compares very favorably with similar test instruments at three times the price. In an OC-3/STM-1, all 84 T1s or all 63 E1s can be identified and processed in transmit and receive modes. In an OC-12/STM-4, all 336 T1s or all 252 E1s can be identified and processed in transmit and receive modes.

The hardware can also be easily configured / programmed for delaying of ATM Cells or PPP packets. The card's multiple connectivity using PCIe, Gigabit Ethernet (GigE), USB 2.0, and onboard DDR2 memory makes it suitable for various applications.

For more details, refer <u>LightSpeed1000™</u> webpage.

Main Features

Hardware ED-137 Signaling Simulation

- *Multiple cards per system for super high capacity monitoring and test system
- High performance x4 PCIe interface with optimized DMA to perform Rx and Tx packets to/from PC memory
- Hardware based precise time-stamping of cells with 10 nsec resolution, 1 ppm accuracy

Analyzer Features

- Software selectable OC-3 / OC-12, or STM-1 / STM-4 for Unchannelized ATM, PoS or Transparent Traffic, and Channelized T1, E1, T3, E3 traffic
- API Toolkit to develop user specific applications



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Main Features (Contd.)

Traffic

- *Wirespeed processing of ATM, PoS or RAW data for Tx and Rx for both ports
- *Precisely emulates packet delays that occur over SONET/SDH carrying ATM or PoS traffic, delay is adjustable from 1 ms to maximum of 500 msec
- Ability to capture/playback to/from disk at full rate in both directions for all ports for detailed offline analysis
- Simultaneous synchronous capture or transmit is possible on all optical ports
- Comprehensive transmit/receive testing capabilities; transmitting and verifying data with incrementing sequence numbers with each packet/cell

BERT

• Easy to use and flexible Bit Error Rate Test (BERT) application for ATM, POS, and RAW

Protocol Testing

• ATM (AAL2, AAL5) Protocol Analyzer, UMTS Protocol Analyzer, PPP (IP and higher layer protocols) Protocol Analyzer

*PCIe card only

PoS Analyzer– Packet Over SONET / SDH

Overview

PoS, or Packet over SONET / SDH—OC-3/STM-1 and OC-12/STM-4 is supported at full rates over. Access, capture, analysis, and emulation of PPP and HDLC, all carrying IP traffic in real-time makes this card useful to many applications including routing, deep packet inspection, and other internet traffic applications.

PoS Protocol Analysis

PPP Analyzer can be used to capture a host of PPP protocols exchanged between the two nodes over SONET/SDH link. User can obtain detailed analysis of higher later protocols (IP, TCP, UDP, HTTP, FTP, POP3 etc.) and can perform various statistics measurements. Integrated Packet Data Analysis (PDA) in Real-time PPP Analyzer is an outstanding tool for live monitoring of VoIP traffic. It can segregate IP traffic into SIP / H323 / MEGACO / MGCP calls and collects statistics, CDRs, ladder diagrams, and a host of other useful information about VoIP calls.

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Dev	TS	Frame#	TIME (Relative)	Len	Error	PPP Layer3Prot	Source IP Addr	Destination IP Ad	UDP Source	UDP Destination	1
$\sqrt{2}$	0	0	00.00.00.000000000	1030		Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	Τ
/ 2	0	1	00:00:00.000013770	1030		Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
/ 2	0	2	00:00:00.000027640	1030		Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
1 2	0	3	00:00:00.000041410	1030		Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
/ 2	0	4	00:00:00.000055270	1030		Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
/ 2	0	5	00:00:00.000069050	1030		Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
/ 2	0	6	00:00:00.000082910	1030		Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
12	0	7	00:00:00.000096770	1030		Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
/ 2	0	8	00:00:00.000110550	1030		Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
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Figure: PPP Protocol Analyzer

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PoS Port Configuration

PoS Port Configuration allows users to select FCS type, control FCS stripping on Rx and FCS appending on Tx.

Attribute	Port 1	Port 2	
Rx FCS Bit Count	32 bits	32 bits	
Rx FCS Octets Present	strip	strip	
Tx Append FCS	32 bits	32 bits	
Port 1 32	? bits		
) bits		
na	ne		

Figure: PoS Port Configuration

PoS BERT

Support for the following PRBS Patterns: $2^9 - 1$, $2^{11} - 1$, $2^{15} - 1$, $2^{20} - 1$, $2^{23} - 1$, $2^{29} - 1$, $2^{31} - 1$, all one's, all zero's, alternate ones and zeros, user-defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10^-1 to 10^-9, status for pattern sync, bit errors counters, and packet rate and packet gap configuration options, configurable header lengths and header information.

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Por File View Windows Help								_ 8 X
Ports: Port	t1 • _							
Configurations	Tx Config		Ψ×	Rx Config				Ψ×
Port 1	TA COILING			; Ka coning				
	Port Selection Port 1	🔻 🗹 Tx Rx coupled set	tings	Port Selection Port 2 V	Tx Rx coupled settings			
Tx Config		_						
Rx Config	Layer PPP IP	PayLoad Traffic Rate Im	pairments	Layer PPP IP Pay	Load			
Results	IP Selection - IPv4	Y		BERT Configuration		Sync Declare Settings	_	
Statistics	In Delocation Thomas						-	
Port 2	Src TP Address	192 . 168 . 1 . 11	-	BER Pattern 2^9-1	T	Sync Achieve Declare Count 64		
🖃 🥣 Bert - Rx	area rission [172 - 100 - 1 - 11		31 User Defined Pat	tern 0 Length	Sync Loss Declare Count 1	1	
Tx Config	Dest IP Address	192 . 168 . 1 . 10		51 User Defined Pad				
Rx Config Results			-		3 💌 bits	Sync Loss Declare Window 1000		
Statistics	Auto Inc Dest IP	Range 10		All Ones All Zeros	D	Restore Default		
	Results		Ψ×	Statistics				Ψ×
	Kesuics			Statistics				Ť ^
F	Port Selection Port 1	Reset Clear LE	D History Insert Error	Port Selection Port 1	Reset Rx			
	Bert Status			Tx	Values	Rx	Values	
	R× No Traffic	Not Active		Frame count	-	Total frame count	925822	
	Sync Loss	Not Active		Byte count	-	IPv4 frame count	925822	
	Bit Error	Not Active				IP checksum error count	0	
	Out of Sequence Packet	Not Active				IPv6 frame count	0	_
L						Non IP test frame count	0	
	Bert Statistics	Values				IP data over IP layer frame count	0	
E	BERT Status	SYNC		-		UDP data over IP layer frame count TCP data over IP layer frame count	925823 0	
	Test Time	00:00:32				ICP data over IP layer frame count	0	
	No Rx Data Count	0				IGMP data over IP layer frame count		
1	No Rx Data Seconds	0				IGRP data over IP layer frame count		
	Bits Received	259135200				Other data over IP layer frame count		
	Bit Error Count	0				UDP checksum error frame count	0	
		0.0000E+000				UDP frame count	0	
	Bit Error Seconds	0				Non UDP test frame count	0	
	Out Of Seq. Count	0						
	Sync Loss Count Sync Loss Seconds	0						
	Error Free Seconds	33						
	citor tree seconds	55		L				_

Figure: PoS BERT

PoS Tx / Rx Test

An emulation and test capability that transmits fixed, random, or variable lengths test packets and checks packets on receive at a user specified data transmission rate.

POS Tx/Rx Test				×
Tx Port Rx Port	- Statistics		-Rx	
	Packets	5 973	Packets	5 841
Length without FCS Fix/Var Packet Length —				
Min: 20 Fixed Var. Increment	Bits/Sec	4 070 880	Bits/Sec	3 980 416
Max: 1000 Var. Random	Pkts/Sec	990	Pkts/Sec	968
Fixed: 203	Percent	2.739	Percent	2.678
Tx Config (max 148.608 Mbps) Packets/Sec 1000	Results Rx Seq Erro	or Count 0		
Bits / Sec Percent	Tx Overru	n Count	0 Rx Underrun Co	unt0
4 080 000 2.767				
Prepend Fixed Length Header Octets (Hex)	Rx Error Statistic Bu	uckets		
	Packet Length	Total Co	unt Error Coun	t Err %
	1-10			0.000
	11-50			0 0.000
Rx Error Statistic Length Buckets (space separated)	51-200			0 0.000
10 50 200 500 2000 None	501-2000			0 0.000
· · · · · · · · · · · · · · · · · · ·	2001-8000	2 .		0 0.000
Default			-	
Pause Tx				
		1		
Start Stop Insert Error	Reset Errors	Exit		

Figure: PoS Tx/Rx Test



ATM Analyzer– Asynchronous Transfer Mode Over SONET / SDH

Overview

ATM over SONT/SDH— OC-3/STM-1 and OC-12/STM-4 is supported at full rates. Access, capture, analysis, and emulation of ATM cells at wirespeed make this interface capability applicable for wide ranging next generation networks.

ATM Protocol Analyzer

ATM Analyzer is used to analyze and view ATM protocols across the U-plane for both NNI and UNI interface carrying AAL0, AAL2 and AAL5 traffic.

UMTS Protocol Analyzer

UMTS analyzer is capable of capturing, decoding and performing various test measurements across various interfaces i.e. lub, lur, luCs and luPs interfaces of the UMTS network. In addition, it supports ATM as the transport layer. It helps in fault diagnosis and troubleshooting UMTS network.

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Dev TS	Frame#	TIME (R	(elative)	Len	Enor	VPI VI	I PT	OSF	AAL Type	Frame Ty	CID	U	UUI	CPI	ę,
2 30	9	00.00.00.033	999500	53		1 56	1		AAL5	CPS-Frame				0	
2 30	10	00:00:00.034	880625	53		1 72	1		AAL5	CPS-Frame				0	
2 30	11	00:00:00.050	999250	149		1 56	0		AAL5	CPS-Frame				0	
2 30	12	00:00:00.053	439458	101		1 40	0		AAL5	CPS-Frame				0	
2 30	13	00:00:00.055	400458	101		1 40	0		AAL5	CPS-Frame				0	
2 30	14	00:00:00.061	400500	53		1 40	1		AAL5	CPS-Frame				0	
2 30	15	00:00:00.062	040917	53		1 40	1		AAL5	CPS-Frame				0	
1 1	10	00.00.00 000	300038	61		1 0/			4410					0	-
M Frame GFC VPI VCI PT CLP	Data ATH I	ayer		00.0339999	= Sc: = 00 = 1 = 56	rambled 00	0 0001. 000 0000 (1))	00)						
GFC VPI VCI PT CLP Payload Padding CPCS Use	Data ATM I AALS r-to_User		(CPCS-I	PDU) Layeı	- Sc: - 000 - 1 - 56 000 - 000	rambled 00 (00 (0 001. 0 F000000	(0) 00 0001. 00 0000 (1) (0) 01000000 0280001 (0) (0)	0011 10	0	00004010	SF9FI	FFE05	FFE290	0000	
IM Frame GFC VPI VCI FT CLP Payload Padding CPCS Use Conson P. Length	Data ATM I AALS r-to_User	ayer Reassembly Indication ator (CPI)	(CPCS-I	PDU) Layeı	- Sc: - 000 - 1 - 56 000 - 000	rambled 00 (00 001. F000000 1020001 000000 000000	(0) 00 0001. 00 0000 (1) (0) 01000000 0280001 (0) (0)	0011 10	0	00004010	5F9FI	FE05	FFE290	0000	1

Figure: ATM Protocol Analyzer

ATM Configuration

ATM Configuration allows user to either pass or drop the Idle cells at the receiving stream.

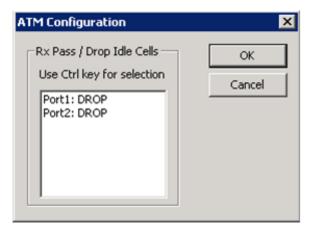


Figure: ATM Port Configuration

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ATM BERT

Support for the following PRBS Patterns: 2⁹ -1, 2¹¹ -1, 2¹⁵ -1, 2²⁰ -1, 2²³ -1, 2²⁹ -1, 2³¹ -1, All one's, all zero's, alternate ones and zeros, user defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10⁻¹ to 10⁻⁹, HEC error insertion, on receive filtering is provided for idle cells, GFC, VPI, VCI, CL, and PT cells, statistical details for total cells, valid cells, idle cells, filtered cells, and filtered out cells.

- ATM Bert - [Untitled]										_ 🗆 🗵
- File View Windows I	Help									_ 8 ×
×	Ports: Port 1 •	-								
Configurations	Tx Config			4 ×	Rx Config					4 ×
Port 1 Trx Config Results Results Port 2 Port 2	Port Selection Port 1 If If R.R. coulded settings Layer ATM Header PayLoad Traffic Rate Impairments BERT Configuration BERT Configuration BERT Configuration Impairments 31 User Defined Pattern 0 Layer All Ones All Zeros 0					ort 2 To To ar PayLoad tion 15-1 Defined Pattern	x Rx coupled settin	Sync Declare Sett Sync Achieve Dec Sync Loss Dec ts Sync Loss Decla	lare Count 64	
	Invert Pattern									
1	Results			4 ×	Statistics					ά×
	Port Selection Port 1	▼ Reset Clea	r LED History Insert Error		Port Selection	ort 1 💌 Rese	t Rx			
	Bert Status				Tx	Values		Rx	Values	
Start Tx Stop Tx	Rx No Traffic	Not Active			Frame count			Total cell count	2912921	
Start Rx Stop Rx	Sync Loss Bit Error	Not Active Not Active			Byte count	-		Idle cell count BER test cell count Filtered out cell count HEC error count	0 2912922 0 0	
	Bert Statistics	Values								
	BERT Status	SYNC			L					
	Test Time	00:01:21			L					
	No Rx Data Count No Rx Data Seconds	0								
	Bits Received	1105843832								
	Bit Error Count	0								
	Bit Error Count Bit Error Rate	0.0000E+000								
	Bit Error Count Bit Error Rate Bit Error Seconds	0.0000E+000 0								
	Bit Error Count Bit Error Rate	0.0000E+000								

Figure: ATM BERT

ATM Tx / Rx Test

An emulation and test capability that transmits ATM test cells and / or analyzes the received cells at a user specified data transmission rate

ATM Tx/Rx Test	<u>×</u>
Tx Port Rx Port User/Network Interface Tx Port Num C NM ATM Header Fields GFC 5 Generic Flow Control (0-15)	
VPI 20 Virtual Path Identifier (0-255) VcI 655 Virtual Channel Identifier (0-65535) PT 0 Payload Typel (0-7)	Bits/Sec 12 623 328 Bits/Sec 0 Cells/Sec 29 772 Cells/Sec 0
CLP Cell Loss Priority (0-1)	Percent 8.429 Results Rx Seq Resync Count Rx Seq Error Count Tx Overrun Count P Rx DTE Error Count P

Figure: ATM Tx/Rx Test

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Other Applications in LightSpeed1000[™] Analyzer

Record, Playback Packets and Cells

These modules allow users to transmit and capture packets from file or to a file over OC-3/STM-1 and OC-12/STM-4 interfaces. Offline utility can convert it into GL's HDL file format or PCAP format.

Transmit Packets from File

- Transmits packets / cells from the file
- Packets can be transmitted either continuously, limited by number of packets/cells, or till the end of file (EOF)
- Transmit packets/cells at a user configurable rate
- Transmits on the same port as captured, swaps ports or uses a specified port
- Provides the statistics of the transmitted cells at both line level and payload level
- Transmit packets synchronously on multiple boards

Receive Packets to File

- Hardware provided **versatile multiple filters** can be applied to incoming data on each individual port to allow traffic of interest only. ATM and PoS traffic can be filtered at hardware level to target traffic of interest only
- Allows Wirespeed capture of all payload from SONET/SDH envelop transparent of transport level
- Captures the received packets synchronously on multiple boards into a file up to hard drive capacity
- Packets can be captured continuously (till user manually stops the capture or up to hard drive capacity) or limited by a specified size in MB, a packet count, or a specified time limit

	Transmit Ports	Input File			
	- 2	D:\LIGHT_SE	PEED TEST DATA\atrm\o	:3 1000 paclet	
	-	-Input File Cells		It File Capture Ports	
		1 000		c rile Capture Ports	
	All selected	Transmission Li	insile		
	ports must reside on a single board		and the second	EOF Continuous	
	Tx Config (max 148	Mbps, 350 Kcps) —	File to Tx Port Packe	t Routing	
	Estimated Packet	Length (POS)	C Same C	Swap Ports (0<->1)	
	53		Tx All Packets	on Single Port	
	Cells (Packets) /	Second	Statistics		
		35300	Tx Cells	143 220	
	Bits / Second	14 967 200	Cells/Sec	34 705	
	Percent		Bits/Sec	14 714 920	
	Percenc	9,994	Percent	9.902	
	Start Sto	ip Exit		Board Transmission rt SMB Stop SMB	
	File Output File - File Name -				
	File Output File File Name D:\LIGHT	SPEED TEST DAT	SMB TX Sta		
	File Output File File Name D:\LIGHT Output File	SPEED TEST DAT	Alatrm\test1.DAT	rt SMB Stop SMB	
	File Output File File Name D:\LIGHT	SPEED TEST DAT	Alatrmitest1.DAT	rt 5M8 5top 5M8	I
ive Ports	File Output File File Name D:\LIGHT Output File Output File O0:01:00 Performance Disk Write B	SPEED TEST DAT	Alatrmitest1.DAT	kets C Time C C	
ive Ports	File Output File File Name D:\LIGHT Output File Output File Output File Performance	SPEED TEST DAT	Alatrmitest1.DAT	rt 5MB Stop 5MB	
ive Ports	File Output File File Name D:\LIGHT Output File Output File O0:01:00 Performance Disk Write B 959 092	SPEED TEST DAT	Alatrmitest1.DAT	kets C Time C C	lable
Packets to	File Output File File Name D:\LIGHT Output File Output File O0:01:00 Performance Disk Write B 959 092 File File	SPEED TEST DAT	Alatrmitest1.DAT	kets C Time C C	lable Iverflow Event C

Figure: Receive Packets to File, Transmit Packets from File

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Software Loopback (Rx-To-Tx Memory Loopback)

This application is used for diagnostic purposes. It loops all the received packets / cells from the SONET to the transmitting ports and displays the Tx and Rx information. Memory Loopback application uses both ports on the selected board.

and the second second	nory Loopba	CK	<u>, 11</u>		
X Unde	C	Source (Rx)	ct Port(s) — Destinati 1,2	ion (Tx)	Start
Over	Kuns (ī			Stop
Packe Page	et Mode	Skip Rx and Tx OnT			
 inform 					
Port	Packets	Bytes	Port	Packets	Bytes
	1 004 400	102 940 090	1.2	1 026 420	102 040 000
	1 836 430	102 840 080	1,2	1 836 430	102 840 080
1,2	1 836 430 Avail LB:	102 840 080	1,2	1 836 430	102 840 080
1,2 tx Bytes			1,2	1 836 430	102 840 080
1,2 Ix Bytes Ix Free S	Avail LB:	16	1,2	1 836 430	102 840 080
1,2 tx Bytes fx Free 5 fx Free -	Avail LB: Space LB:	16 52 260 879	1,2	1 836 430	102 840 080

Figure: Memory Loopback

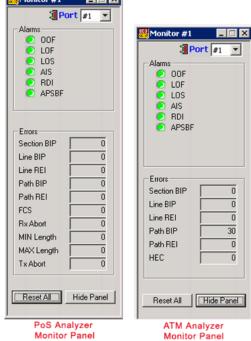
Alarms and Errors Counters Monitoring

The alarms and error monitoring window provided for each of the OC-3/OC-12 port displays detailed status of the communication with the other end.

Hardware LEDs are provided on the card to read line alarms.

Monitored Alarms and error counts include -

- Line errors such as OOF, LOS, LOF, AIS, RDI, and APSBF
- FCS, Rx / Tx Abort, and MIN / MAX Length
- Line, Path, and Section error counts





SONET/SDH RAW (or Transparent) Payload

RAW mode captures or playbacks anything and everything on SONET/SDH. This mode allows capturing/replaying including SONET/SDH Framing and payload. Here payload can be anything, including structured traffic (T1, E1, STS-1, DS3 etc) or unstructured traffic (ATM, PoS, GFP etc). Raw or transparent mode allows direct access to the SONET / SDH payload for BERT, data transmit and receive applications. Current applications include:

- RAW BERT support for the following PRBS Patterns: 2⁹ 1, 2¹¹ 1, 2¹⁵ 1, 2²⁰ 1, 2²³ 1, 2²⁹ 1, 2³¹ 1, all one's, all zero's, alternate ones and zeros, user defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10⁻¹ to 10⁻⁹, status for pattern sync, and bit errors counters
- Wirespeed capture of raw data to hard disk on one or both ports simultaneously. The data is recorded in 64 bytes block with appropriate header
- Playback of recorded data from file at wirespeed on one or both ports
- Alarms and Error monitoring and logging at SONET/SDH level

Performance Counters

Following performance counters are available in the analyzer: Tx Statistics, Rx Statistics, PMC TxRx Statistics, Interrupt Statistics, and DMA Engine. The statistics display two types of counters: board counters and port counters. The board counters display cumulative counts for all ports on the same board, while port counters display information for each port separately.

DMA TX Inte	💽 Tx Statis	tics				×
s DMA RX Inb Board		Rx Statistics				×
	DOMA ET C					
r L DMA TX Inte m F DMA RX Inb	DMA Enç PC Memc	Board Counters	ş 🛛	Board 1		
r 1 DMA Timer 1	DTE Pack	DMA Engine PC		192 688 918		
Force Statis	DTE GigE	DMA Engine PC DTE Packets	Ie Pgs	3 391 681 192 195 103		
w ł	INTF Gig	DTE GIGE PKTs		192 195 103		
	INTF Gig INTF Gig	INTF GIGE PKTs		3 735 936 685		
1		INTF GigE Error INTF GigE Pkts		3 735 936 685 3 735 936 685		
		INTE GIGE Max		3 735 936 685		
	1	INTF GigE Min L		3 735 936 685		
	Port Cou	1	PMC Tx/Rx	Statistics		
	DTE Pad INTE Pac					
	INTF Errc	Port Counters DTE OC-3/121	Port Counter	s	Port 1	Port 2
	INTF Pac	INTF OC-3/12	TX cells		4 996 949	187 203 069
		INTF OC-3/12	RX idle cells		0/0.050.015	1 100 010 (71
		INTF OC-3/12 INTF OC-3/12	RX cells		960 059 015 187 240 772	1 138 319 674 5 427 366
		INTF OC-3/12	RX HCS error	s	0	4
		Filtered OC-3/				
	J	Filtered OC-3/ Filter OC-3/12				
		Filter OC-3/12	-			
		Elber OC 2112				
esh.						

Figure: Packet Delay Emulation

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Software Loopback (Rx-To-Tx Memory Loopback)

This application is used for diagnostic purposes. It loops all the received packets / cells from the SONET to the transmitting ports and displays the Tx and Rx information. Memory Loopback application uses both ports on the selected board.

		t Port(s)		
× UnderRuns	50urce (Rx)	Destinati	ion (Tx)	Start
OverRuns	ō			Stop
Packet Mode	Skip Rx and Tx OnT	imer (pause >	cmit)	
Page Mode	Flush Tx After Each	Packet Ty (n	acket mode)	
	Flush TX Arter Each			
× information			nation	
cinformation Port Packets	Bytes			Bytes 102 840 080
x information Port Packets	Bytes	Tx inform	nation Packets	
× information Port Packets	Bytes	Tx inform	nation Packets	
× information Port Packets	Bytes	Tx inform	nation Packets	
x information Port Packets 1,2 1 836 430	Bytes 102 840 080	Tx inform	nation Packets	

Figure: Memory Loopback

Packet Delay Emulation for PoS and ATM based traffic

The Network Delay Emulator is an optional application (requires license) provides full duplex delay simulation for PoS and ATM based traffic from 1 ms to 500 ms, with incremental delays of 1 ms. The application combines hardware and software based functions to achieve precision and flexibility. It can emulate packet delays that occur over SONET/SDH carrying ATM/PoS traffic.

With this application, the user can:

- Test the impact of delay and congestion under various real world conditions
- Assess impact of delay on SLA (Service Level Agreements),
- Simulate satellite delay and long Fiber Loops
- Test WAN application performance under deteriorated but repeatable conditions

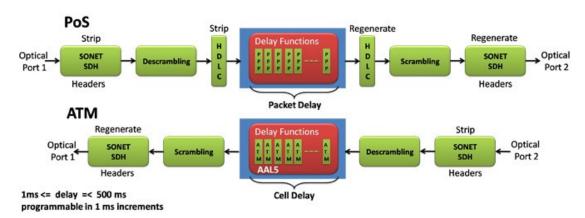


Figure: Packet Delay Emulation

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Supported Protocols

- ATM Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation 1.432
- **PPP over SONET (PoS)** Implements the Point-to-Point Protocol (PPP) over SONET / SDH specification according to RFC 2615 (1619) / 1662 of the PPP Working Group of the Internet Engineering Task Force (IETF)
- OC-3/OC-12/STM-1/STM-4 Transparent Payload Analyzer processes SONET/SDH payload in transparent (RAW) mode without any transport protocols

Specifications

Interfaces:

- 2 x Unchannelized OC-3 / STM-1 / OC-12 / STM-4 Ports (Port 1 Port 2)
- 2 x Channelized OC-3 / STM-1 / OC-12 / STM-4 Ports (Port 3 Port 4)
- Single Mode or Multi Mode SFP support with LC connector

Protocols:

• POS compliance specs - RFC 2615(1619)/1662

Tx Clock

• Internal or Recovered

Alarm LEDs:

• LOS, LOF, User

Bus Interface:

- PCIe Specification
 - 1.2 Compliant
- USB 2.0

Power and Dimensions:

- +12 volts, 3.5 Amps
- 4.2" x 9.2"



Buyer's Guide

Item No	Product Description
<u>LTS100</u>	Lightspeed1000™ - Dual OC-3/12 STM-1/4 PCIe Card
LTS105	Lightspeed1000™ - Portable Dual OC-3/12 STM-1/4 USB Unit
<u>IPN1310a</u>	SFP Transceiver for OC-3/STM-1 and OC-12/STM-4 Optical, LC, Single-Mode, 1310nm
<u>IPN850a</u>	SFP Transceiver for OC-3/STM-1 and OC-12/STM-4 Optical, LC, Multi-Mode, 850 nm or 1310 nm

Item No	Unchannelized Analysis and Emulation Applications Related Software
<u>LTS200</u>	OC-3/STM-1 ATM Monitor, BERT, Tx/Rx Test, RAW
<u>LTS300</u>	OC-12/STM-4 ATM Monitor, BERT, Tx/Rx Test, RAW
<u>LTS201</u>	OC-3/STM-1 PoS Monitor, BERT, Tx/Rx Test, RAW
<u>LTS301</u>	OC-12/STM-4 PoS Monitor, BERT, Tx/Rx Test, RAW
<u>LTS202</u>	OC-3/STM-1 ATM and RAW Record / Playback
<u>LTS203</u>	OC-3/STM-1 PoS and RAW Record / Playback
<u>LTS302</u>	OC-12/STM-4 ATM and RAW Record / Playback
<u>LTS303</u>	OC-12/STM-4 PoS and RAW Record / Playback
<u>LTS204</u>	OC-3/STM-1 ATM Protocol Analysis
<u>LTS304</u>	OC-12/STM-4 ATM Protocol Analysis
<u>LTS206</u>	OC-3/STM-1 UMTS Protocol Analysis
<u>LTS306</u>	OC-12/STM-4 UMTS Protocol Analysis
<u>LTS215</u>	Packet Data Analysis (PDA) for PoS
<u>LTS207</u>	Delay Emulation for OC-3/STM-1 PoS payloads
<u>LTS208</u>	Delay Emulation for OC-3/STM-1 ATM payloads
<u>LTS307</u>	Delay Emulation for OC-12/STM-4 PoS payloads
LTS308	Delay Emulation for OC-12/STM-4 ATM payloads

GL Communications Inc.

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Buyer's Guide (Contd.)

Item No	OC-12 / STM-4 Related Software Related Hardware
<u>LTS501</u>	OC-3/STM-1 RAW
<u>LTS502</u>	OC-12/STM-4 RAW
<u>LTS503</u>	Record Playback for OC-3/STM-1 RAW
<u>LTS504</u>	Record Playback for OC-4/STM-4 RAW
<u>LTS108</u>	Any 16 Ports Channelized License for OC-3/STM-1
LTS116	Any 32 Ports Channelized License for OC-3/STM-1
<u>LTS124</u>	Any 48 Ports Channelized License for OC-3/STM-1
LTS132	Any 64 Ports Channelized License for OC-3/STM-1
LTS164	All Ports Channelized Licenses for OC-3/STM-1 (84x2 for T1, 63x2 for E1)

For more details, refer <u>LightSpeed1000™</u> webpage.



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